



Analysis and design of a transimpedance amplifier based front-end circuit for capacitance measurements

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Abstract

In this study, transimpedance amplifier based front-end circuits which can be employed to measure small capacitances were designed, analyzed and simulated using analog electronic circuit simulator. The front-end circuit converts the current flowing through the measured capacitance into a modulated voltage value which contains information regarding the desired capacitance. The frequency-domain, time-domain, stability and noise analyzes were carried out numerically and in simulation environment using a circuit simulator. The analytical, numerical and simulation results can be used to design optimized, precise and stable transimpedance amplifiers with low-noise value. The measured capacitance value was 10 pF which is low enough to simulate various real-world applications. Three commercially available, off-the-shelf operational amplifiers with different peripheral passive components were employed for computer based analysis. The designed transimpedance amplifiers are suitable to connect with capacitance extraction circuits which use analog or digital demodulation techniques.

Keywords Analog design · Capacitance measuring · Front-end circuits · Noise analysis · Transimpedance amplifiers

1 Introduction

Capacitive sensors are used to sense and measure many variables like acceleration, angular velocity, pressure, electric field and fluid level [1]. Their applications can be found in many areas such as accelerometers [2, 3], gyroscopes [4, 5], pressure sensors [6, 7], humidity sensors [8] or liquid level measurement circuits [9]. The capacitance of a capacitive sensor changes according to the physical signal variation. The detection circuit produces an output signal proportional to this change. Therefore, the capacitance value and its changing must be detected accurately to ensure better and reliable measurements. The overall measurement performance can be improved with the proper selection of circuit components [10]. This paper's main aim is to aid the capacitance measuring circuit parameters

selection by investigating optimum performance metrics such as gain, stability, settling time and noise.

A capacitance measuring circuit topology mainly consists of three main parts: the excitation signal, the sensing part, and the readout circuit. The excitation input is applied to stimulate the measured capacitance so that a response output signal is produced. The excitation signal is generally a voltage source, and its waveform can be a sinusoid or a square wave depending upon the type of application it is used. The second part is the sensing part which includes the capacitance to be measured. Usually, there is only one capacitance or two capacitances in differential form [11]. The final part is the readout circuit which acquires the sensed signal and conditions it by means of analog or digital demodulation methods [12]. An example of an analog signal processing block diagram

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is shown in Fig. 1 [13]. The sensing part in Fig. 1 is in differential capacitance form while the readout circuit uses synchronous demodulation for capacitance extraction. The multiplication operation in the demodulation part can be implemented using analog multipliers or analog switches while low-pass filtering can be realized by operational amplifiers (OPAMP) along with passive components [14]. The output signal is a voltage that is in proportional with the differential capacitance value.

On the other hand, Fig. 2 shows a general digital signal processing diagram built for the purpose of capacitance measurement. Field Programmable Gate Arrays (FPGA) [10, 15], Complex Programmable Logic Devices (CPLD) [16] or Digital Signal Processors (DSP) [17] could serve as the signal processing platform. The aforementioned platforms can generate the required excitation signal by digital means. A digital-to-analog converter (DAC) converts the digital signal to the analog stimulus signal. The low-pass filter removes the effects of high frequency noise in the produced excitation signal, and provides a smooth driving signal for the sensing part. Transimpedance Amplifier (TIA) acts as the analog front-end circuit by converting the sensed current into voltage. The output signal of the TIA is then filtered from the noises caused by the analog front-end circuit, and is sampled by an analog-to-digital converter (ADC). The sampled signal data should be demodulated using digital methods so that the capacitance value can be acquired. Digital phase sensitive demodulation

[18–20], recursive demodulation [16, 21, 22], digital recursive demodulation based on Kalman Filter [23], information-filtering demodulation [24] are some examples of digital demodulation techniques suggested in the literature.

Both analog and digital signal processing platforms require an analog front-end interface to obtain and process the modulated signal. As a current-sensing topology, TIA based analog front-end interface is the most suitable circuit topology due to the being insensitive to the effects of stray capacitances arising from internal geometry or external connections. Furthermore, this TIA topology offers high signal-to-noise ratio (SNR) [10]. Stray capacitance effects are eliminated by the fact that the potential over the stray capacitor is kept zero by the virtual ground.

The measurement circuit's performance can be improved by a careful design of the TIA. An optimized TIA design should have the following features: low total noise at the output, short settling time, increased stability, and high voltage gain. In fact, when the literature is reviewed [16, 18, 25–30], it is noticed that the TIA design parameters are generally selected intuitively without optimizing the features mentioned above. This paper aims to evaluate the TIA based front-end circuit's various performance parameters. With the help of the performance evaluation, the design parameters of the TIA can be chosen properly. In this work, it is demonstrated that a decent TIA design may require to make trade-offs between different performance metrics.

Fig. 1 Analog signal processing block diagram

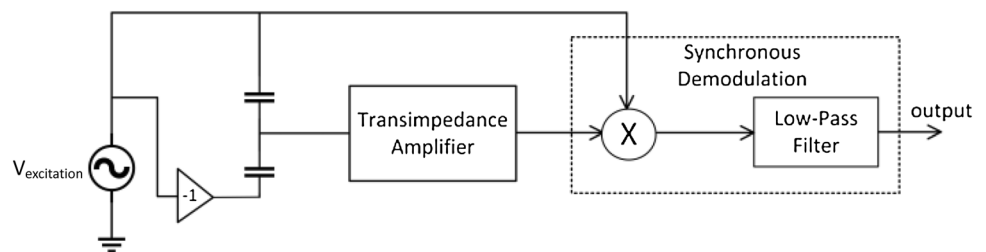
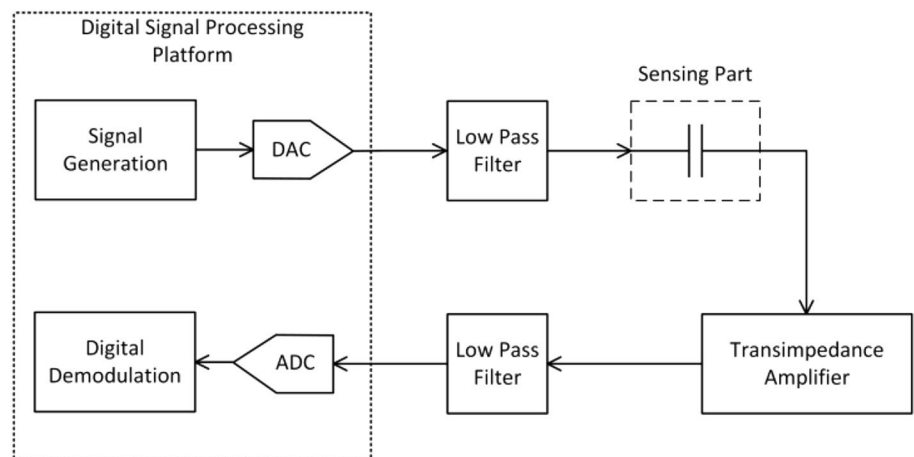


Fig. 2 Digital signal processing block diagram



The next section of the work introduces the TIA topology and contains four different types of circuit analyzes. Stability analysis, frequency-domain analysis, time-domain analysis and noise analysis are given for the TIA, respectively. In the subsequent section of the work, numerical and simulation results are presented and discussed. Finally, the conclusion of the study is given.

2 Materials and methods

2.1 Transimpedance amplifier topology

A typical topology of a TIA used to measure an unknown capacitance is shown in Fig. 3. This circuit functions as a capacitance-to-voltage convertor. The current flowing through the unknown capacitance C_x is converted to voltage by the feedback impedance. C_{in} represents the internal input capacitance of OPAMP which is created by the differential-mode input capacitance and common-mode input capacitance. R_f is the feedback resistor while C_f is the feedback capacitor which is connected to ensure the stability of the output. V_{in} is the sinusoidal excitation input signal and V_{out} is the phase and amplitude modulated version of the input signal. The output signal is modulated due to the effects of operational amplifier’s internal parameters and peripheral passive components. C_x is the only unknown parameter of the output voltage. Thus, its value can be found using the known parameters of the circuit after an analog or digital demodulation process is implemented.

2.2 Stability analysis

In order to prevent oscillations at the output voltage, the feedback capacitor C_f works as a compensation component and ensures the stability of the system. The minimum value of C_f can be calculated [31] as in Eq. (1).

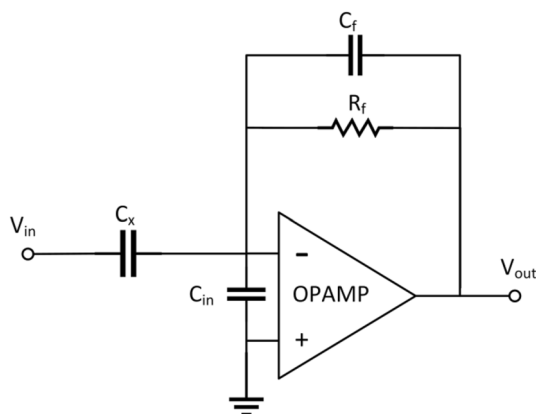


Fig. 3 Transimpedance amplifier topology

$$C_f \approx \sqrt{\frac{C_x + C_{in}}{2\pi R_f f_{GBWP}}} \tag{1}$$

where f_{GBWP} is OPAMP’s gain-bandwidth product. Equation (1) is derived from the intersection frequency of the open-loop gain of the OPAMP and the feedback factor. The feedback factor is the ratio of the output signal value to its feedback signal value at the inverting input of the OPAMP. Selection of a larger valued feedback capacitor seems reasonable to keep the circuit stable. However, larger valued feedback capacitor narrows the available bandwidth and increases the settling time.

2.3 Frequency-domain analysis

The ratio of the output voltage to the input voltage for the TIA given in Fig. 3 can be expressed in the frequency-domain as in Eq. (2).

$$G(j\omega) = \frac{-j\omega C_x R_f}{1 + \frac{1}{A_v(f)} + j\omega \left(C_f R_f + \frac{R_f C_f}{A_v(f)} + \frac{C_{in} R_f}{A_v(f)} + \frac{C_x R_f}{A_v(f)} \right)} \approx \frac{-j\omega C_x R_f}{1 + j\omega C_f R_f} \tag{2}$$

where A_v is the open-loop gain of the OPAMP and ω is the natural frequency of the input signal. Actually, A_v is a frequency-dependent parameter and its value decreases with increasing frequency. The value of open-loop gain at the operating frequency of the TIA is much larger than that of the quantities it is compared with. Therefore, the transfer function can be approximated as given in Eq. (2). Further simplification is possible as in Eq. (3) if the condition $\omega^2 R_f^2 C_f^2 \gg 1$ is met.

$$G(j\omega) = -\frac{C_x}{C_f} \tag{3}$$

Equation (3) implies that the output voltage does not depend on the operating frequency and it has a fixed 180° phase shift with the input [30]. Also, the output amplitude is directly proportional with the measured capacitance C_x .

2.4 Time domain analysis

Time-domain or transient analysis of a TIA is required to evaluate the circuit’s dynamic behavior. When a unit-step signal is applied to the input, the output voltage in Eq. (2) can be expressed as in Eq. (4) assuming the capacitors are fully discharged initially.

$$V_{out}(s) = \frac{\left(-\frac{C_x}{C_f}\right)}{s + \frac{1}{R_f C_f}} \tag{4}$$

Taking the inverse Laplace transform of both sides in Eq. (4), time-domain equation for the unit-step response can be written as in Eq. (5).

$$V_{out}(t) = -\frac{C_x}{C_f} e^{-\frac{t}{R_f C_f}} \tag{5}$$

The output voltage given in Eq. (5) is initially equal to $(-C_x/C_f)$ and goes to zero volts. The settling time of this circuit is defined as the duration until the steady-state error falls below 1%. Thus, the settling time equals to $4.6R_f C_f$ where $R_f C_f$ forms the time constant. The settling time of the circuit must be adjusted carefully for better dynamic behavior.

2.5 Noise analysis

There are multiple noise sources originating from OPAMP's internal operations such as inverting and non-inverting input current noises and input voltage noise. There is another noise source called thermal noise emerging from the feedback resistor R_f [32]. The noise sources are independent from each other so that they can be added using root sum of squares (RSS). OPAMP's noise data should be acquired from its datasheet. The noise sources are generally defined as spectral densities that their units are usually given in nV/ $\sqrt{\text{Hz}}$ or pA/ $\sqrt{\text{Hz}}$. In order to find the root-mean-square (RMS) value of the noise at the output, the

spectral density must be integrated over the equivalent noise bandwidth. The TIA's noise model including all noise sources is depicted in Fig. 4.

The noise model in Fig. 4 illustrates four uncorrelated noise sources. The OPAMP's internal noises i_{n1} , i_{n2} and V_n represent inverting input current noise, non-inverting input current noise and input voltage noise spectral densities, respectively. These noise sources are made up of 1/f noise where the noise spectral density is inversely proportional to frequency and the white noise where the spectral density is constant [33]. V_R is the thermal noise spectral density generated by the feedback resistance due to the motion of the electrons and can be expressed as in Eq. (6).

$$V_R = \sqrt{4kTR_f} \tag{6}$$

where k is the Boltzmann's constant (1.38×10^{-23} J/K), T is the temperature ($^{\circ}\text{K}$) and R_f is the value of the feedback resistance (Ohms). In order to find the total output referred noise, Table 1 lists the summary of noise sources, their spectral densities, noise gains and noise bandwidths.

The feedback resistor's noise spectral density is given in Eq. (6) and its noise gain is equal to unity. The noise bandwidth of R_f can be defined as the multiplication of the brick wall factor (K_n) and the transconductance bandwidth. The noise bandwidth of R_f is the intersection frequency of the OPAMP's open-loop gain curve with the noise gain. Also, the noise gain of the inverting input current noise is the gain seen at the inverting input of the OPAMP. Its noise bandwidth is constrained by the TIA's transconductance bandwidth and the brick wall factor. On the other hand, the noise contribution of i_{n2} to the output is negligible. To sum up, any noise source's contribution to the output can be found by the generic formula given in Eq. (7).

$$V_{noise_{RMS}} = (\text{Spectral Density}) * (\text{Noise Gain}) * \sqrt{\text{Noise Bandwidth}} \tag{7}$$

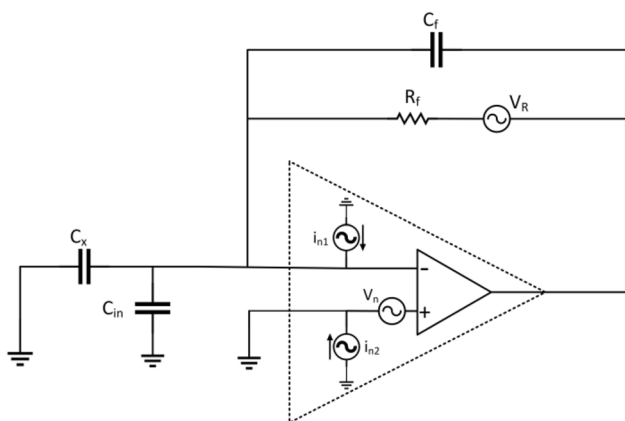


Fig. 4 Transimpedance noise model

Table 1 Noise sources, noise gains and equivalent noise bandwidths for transimpedance amplifier

Noise source	Noise source's spectral density	Noise gain	Noise bandwidth
Feedback resistor (R_f)	$V_R = \sqrt{4kTR_f}$	1	$\frac{K_n}{2\pi R_f C_f}$
OPAMP's input voltage noise	V_n	$\frac{1+sR_f(C_f+C_{in}+C_x)}{1+sR_f C_f}$	$K_n f_{GBWP} \frac{C_f}{C_f+C_x+C_{in}}$
OPAMP's inverting input current noise	i_{n1}	$\frac{R_f}{1+sR_f C_f}$	$\frac{K_n}{2\pi R_f C_f}$
OPAMP's non-inverting input current noise	i_{n2}	No gain	-

3 Results and discussion

3.1 Component selection

First of all, the unknown capacitance C_x was chosen as 10 pF which makes this TIA useful for many applications such as measurement of liquid-level, pressure meters or accelerometers [34]. The input capacitance value depends on the OPAMP used for the design. Minimum value of compensation capacitor can be selected using the Eq. (1). The low-noise OPAMP AD8066 from Analog Devices was employed for the stability, frequency-domain and time-domain simulations. However, the noise simulations were carried out for three different types of OPAMPs. Linear Technology's LTC6268 and Texas Instrument's OPA380 were also simulated to evaluate the noise performances

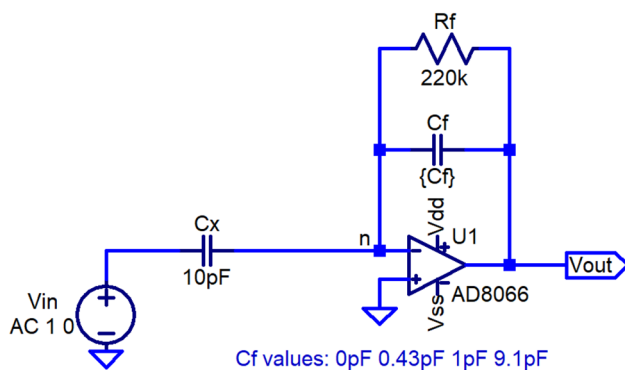


Fig. 5 TIA simulation in LTSPICE

of different OPAMPs. A free Simulation Program with Integrated Circuit Emphasis (SPICE) software called LTSPICE was used to perform all simulations.

3.2 Stability analysis simulations

The TIA circuit is depicted in LTSPICE environment as in Fig. 5. The simulations were carried out for a fixed value of 220 k Ω feedback resistance and various values of feedback capacitance.

Minimum value of the feedback capacitor is calculated 0.43 pF to keep the system stable. Four different values of feedback capacitance were selected to evaluate the effect of the value of C_f on the stability. Figure 6 shows AD8066's open loop gain and the feedback factors of various feedback capacitors. When the feedback capacitor is not connected, the rate-of-closure (ROC) between the open-loop gain curve and the feedback factor curve is equal to 40 dB/decade. The ROC can be defined as the absolute difference of slopes between the two curves. A stable system should have a ROC equal to or less than 20 dB/decade. When C_f is selected as 0.43 pF, the ROC is equal to 20 dB/decade which implies that the system is optimally stable. Selection of a larger valued feedback capacitor makes the system more stable by reducing the ROC as shown in Fig. 6.

3.3 Frequency-domain analysis simulations

The frequency-domain analysis was performed using previous circuit values. Figure 7 indicates the AC Analysis results for various C_f values. This simulation results show that lower C_f provides larger voltage gain as expected from

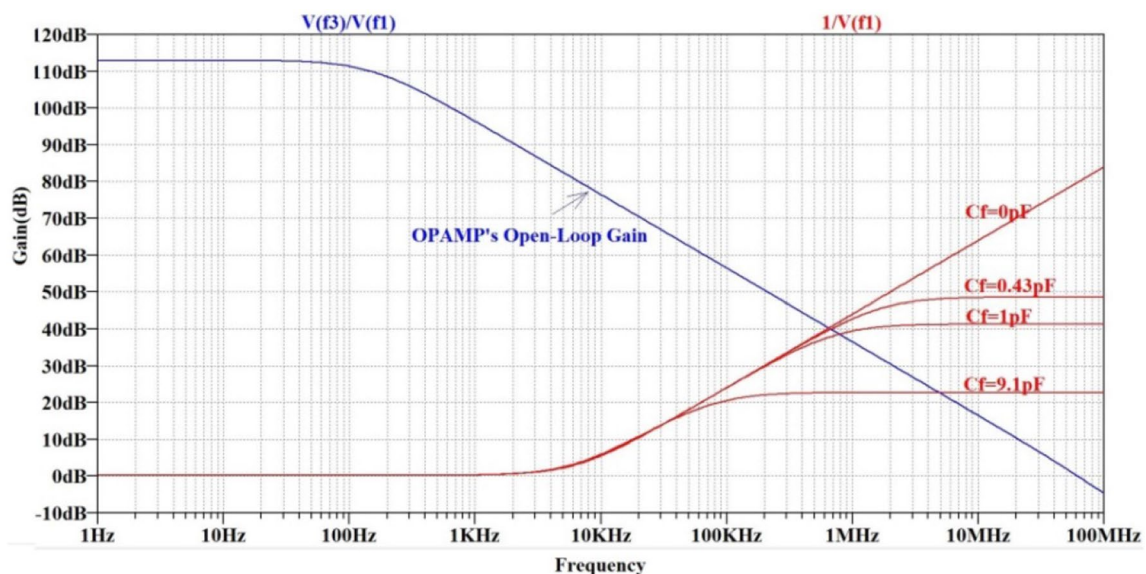


Fig. 6 Stability analysis of TIA for different C_f values

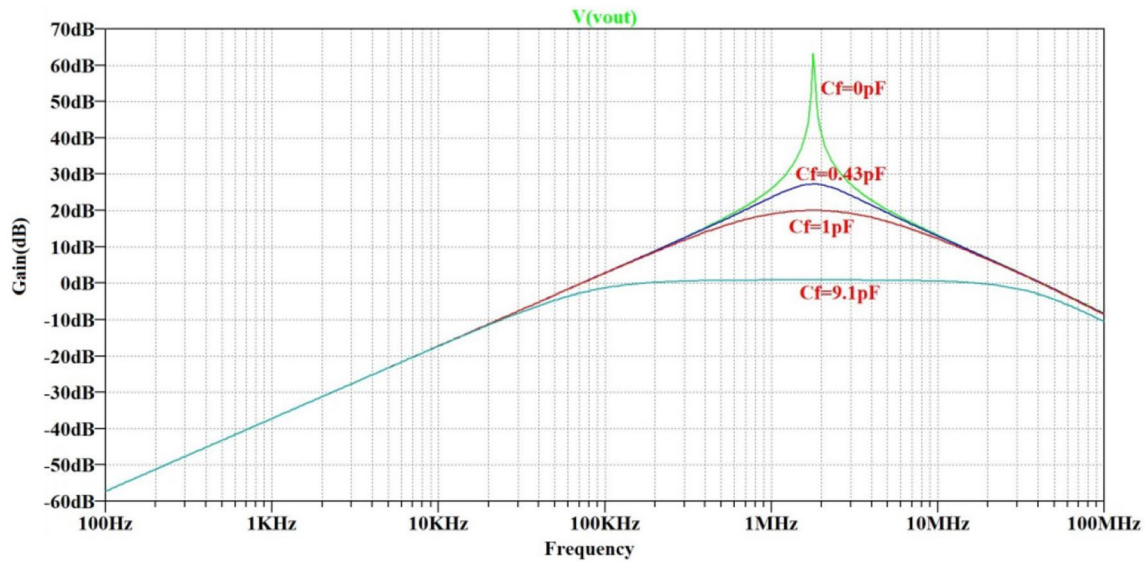


Fig. 7 Frequency-domain analysis of TIA for different C_f values

Eq. (2). At 1 MHz operating frequency, the voltage gain is 26.05 dB for $C_f = 0\text{pF}$ while it is 0.8 dB for $C_f = 9.1\text{pF}$. However, as previously stated, low feedback capacitor values may cause instability. For example, even a small change in the frequency of the input signal may cause a significant change in the voltage gain for low C_f values.

3.4 Time domain analysis simulations

In order to analyze the circuit in time-domain, a unit-step input signal was applied at $1\ \mu\text{s}$. The response of the circuit for different C_f values is observed for $5\ \mu\text{s}$ as shown

in Fig. 8. If there is no feedback capacitor is connected, the output voltage oscillates. If $C_f = 0.43\text{pF}$ is the feedback capacitor, the system is optimally stable. There occurs an overshoot and small ringing at the output. It can also be observed that higher C_f values cause fewer oscillations at the cost of increasing the settling time.

All simulations were performed again for $R_f = 1\ \text{M}\Omega$ and $R_f = 2.2\ \text{M}\Omega$ without changing the feedback capacitor values. Table 2 shows the stability condition, the settling time, and the voltage gain at 1 MHz operation frequency for three different feedback resistance values. The stability condition can be met with lower feedback capacitances if

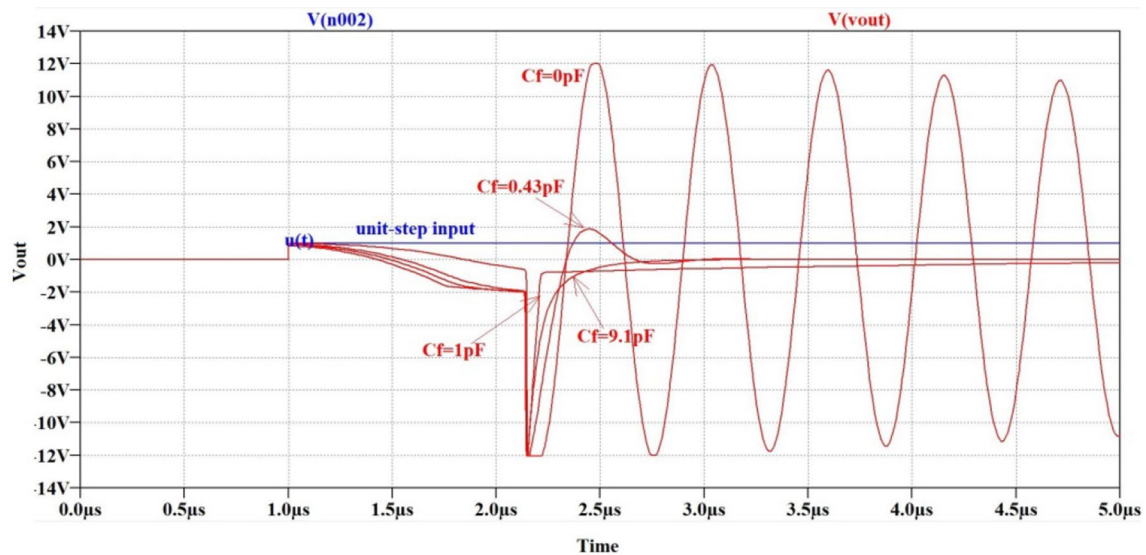


Fig. 8 Time domain analysis of TIA for different C_f values

Table 2 Summary of stability, time domain and frequency domain analyzes for TIA

C_f (pF)	$R_f=220\text{ k}\Omega$			$R_f=1\text{ M}\Omega$			$R_f=2.2\text{ M}\Omega$		
	Voltage gain (dB)	Stability condition	Settling time (μs)	Voltage gain (dB)	Stability condition	Settling time (μs)	Voltage gain (dB)	Stability condition	Settling time (μs)
0	26.05	Unstable	–	43.58	Unstable	–	36.30	Unstable	–
0.43	23.57	Optimally stable	0.04	27.20	Stable	1.97	26.79	Stable	4.35
1	19.01	Stable	0.10	19.97	Stable	4.6	19.89	Stable	10.12
9.1	0.81	Stable	0.92	0.82	Stable	41.8	0.81	Stable	92.09

higher feedback resistances are employed in the TIA. However, the settling time worsens as the feedback resistance or capacitance value increase. If the circuit is stable, the voltage gain does not change too much with R_f . The gain can be increased by lowering the C_f value without driving the system into instability.

3.5 Noise analysis simulations

A MATLAB script was written to calculate the total output noise in RMS using noise related parameters. It is clear that increase in V_n and i_{n1} result in higher noise voltage at the output. Moreover, using an OPAMP with higher gain-bandwidth product raises the total noise because the equivalent noise bandwidth gets larger as suggested in Table 1. A change in the value of feedback resistance does not produce a change in the total output noise because the feedback resistance sets the transconductance bandwidth of the circuit. The OPAMP with low input capacitance should be preferred in the design to lower the total output noise.

Three different off-the-shelf OPAMPs were used to evaluate the noise performance of the TIA circuit. AD8066, LTC6268 and OPA380 are from different semiconductor manufacturers and they have different noise characteristics. Those OPAMPs are selected for their following features in common: low input voltage and low input current noise spectral densities and low input capacitance. Table 3 summarizes the noise related parameters for the selected OPAMPs.

Numerical analysis was carried out in the developed MATLAB script by using the equations given in Table 1 and using the noise related parameters given in Table 3. Simulation results were obtained using LTSPICE's noise analysis feature. Table 4 shows both numerical and simulation results of the total noise at the output in RMS for $R_f=220\text{ k}\Omega/C_f=1\text{ pF}$ and $R_f=220\text{ k}\Omega/C_f=9.1\text{ pF}$. Numerical and simulation results well agree with each other. The lowest noise was found in the simulation of OPA380. An increase in the value of the feedback capacitance caused

Table 3 Noise related parameters for AD8066 [35], OPA380 [36] and LTC6268 [37]

Noise related parameter	AD8066	OPA380	LTC6268
V_n (nV/ $\sqrt{\text{Hz}}$)	7	5.8	4.3
i_{n1} (fA/ $\sqrt{\text{Hz}}$)	0.6	10	5.5
f_{GBWP} (MHz)	65	90	500
C_{in} (pF)	6.6	1.1	0.55

a decrease in the total output noise due to the reduction in the equivalent noise bandwidth.

4 Conclusion

In this study, a TIA-based front-end circuit for the measurement of 10 pF capacitance was analyzed numerically and in simulation environment. Four different analysis methods were performed to evaluate the performance of the front-end circuit. The results of the stability analysis, the time-domain analysis, and the frequency-domain analysis are tabulated in Table 2 for different R_f and C_f values. The numerical and simulation results of the total noise output are summarized in Table 4 for three different commercial OPAMPs. The feedback capacitor's role in the circuit is found to keep the system stable. Nevertheless, the addition of feedback capacitor may decrease the voltage gain and raise the settling time. If a larger voltage gain is required, the value of feedback resistance can be increased. As a conclusion, there are certain trade-offs between the design parameters and operation performance metrics. The circuit designer should adjust the parameters carefully so that the TIA with desired performance criteria is achieved. The circuit performance requirements mainly depend on application in which TIA is used.

Table 4 The total noise output voltages for AD8066, OPA380 and LTC6268

OPAMP	Total noise voltage (μV)	Total noise voltage (μV)	Total noise voltage (μV)	Total noise voltage (μV)
	Numerical results $R_f=220\text{ k}\Omega$ / $C_f=1\text{ pF}$	Simulation results $R_f=220\text{ k}\Omega$ / $C_f=1\text{ pF}$	Numerical results $R_f=220\text{ k}\Omega$ / $C_f=9.1\text{ pF}$	Simulation results $R_f=220\text{ k}\Omega/C_f=9.1\text{ pF}$
AD8066	303.6	289.9	120.8	114.1
OPA380	259.7	240.5	107.8	99.6
LTC6268	424.5	418.8	180.9	171.4

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

References

- Baxter LK (1997) Capacitive sensors: design and applications. IEEE Press, Piscataway
- Junseok C, Kulah H, Najafi K (2005) A monolithic three-axis micro-g micromachined silicon capacitive accelerometer. *J Microelectromech Syst* 14(2):235–242
- Chau K-L et al (1996) An integrated force-balanced capacitive accelerometer for low-g applications. *Sens Actuators A* 54(1–3):472–476
- Erişmiş MA (2004) MEMS accelerometers and gyroscopes for inertial measurement units. The Graduate School of Natural and Applied Sciences of Middle East Technical University, Ankara
- Aaltonen L, Halonen K (2010) An analog drive loop for a capacitive MEMS gyroscope. *Analog Integr Circ Sig Process* 63(3):465–476
- Ko WH, Wang Q (1999) Touch mode capacitive pressure sensors. *Sens Actuators A* 75(3):242–251
- Akar O, Akin T, Najafi K (2001) A wireless batch sealed absolute capacitive pressure sensor. *Sens Actuators A* 95(1):29–38
- Kang U, Wise KD (2000) A high-speed capacitive humidity sensor with on-chip thermal reset. *IEEE Trans Electron Devices* 47(4):702–710
- Reverter F, Li X, Meijer GC (2007) Liquid-level measurement system based on a remote grounded capacitive sensor. *Sens Actuators A* 138(1):1–8
- Xu L et al (2015) Performance analysis of a digital capacitance measuring circuit. *Rev Sci Instrum* 86(5):054703
- Reverter F, Casas Ö (2010) Interfacing differential capacitive sensors to microcontrollers: a direct approach. *IEEE Trans Instrum Measure* 59(10):2763–2769
- Li J, Ferrari G (2018) Capacitance spectroscopy of semiconductors. Jenny Stanford Publishing, New York
- Senturia SD (2001) *Microsystem design*. Kluwer Academic Publishers, New York, p 689
- Chen D et al (2010) Design of impedance measuring circuits based on phase-sensitive demodulation technique. *60(4):1276–1282*
- Carminati M. et al. (2012) Compact FPGA-based elaboration platform for wide-bandwidth electrochemical measurements. In: 2012 IEEE international instrumentation and measurement technology conference proceedings
- Sun S et al (2017) A high-speed digital electrical capacitance tomography system combining digital recursive demodulation and parallel capacitance measurement. *IEEE Sens J* 17(20):6690–6698
- Tiapkin MG, Balkovoi AP (2017) High resolution processing of position sensor with amplitude modulated signals of servo drive. In: 2017 IEEE conference of russian young researchers in electrical and electronic engineering (EIConRus)
- Xu L et al (2013) A digital switching demodulator for electrical capacitance tomography. *IEEE Trans Instrum Meas* 62(5):1025–1033
- Xuehui Z, Huaxiang W (2008) Digital phase-sensitive demodulation in electrical capacitance tomography system. In: 2008 7th World Congress on Intelligent Control and Automation
- Huaxiang W, et al. (2008) Digital signal processing in electrical capacitance tomography. In: APCCAS 2008—2008 IEEE Asia Pacific conference on circuits and systems
- Sun S et al (2018) A recursive demodulator for real-time measurement of multiple sinusoids. *IEEE Sens J* 18(15):6281–6289
- Xu L, Zhou H, Cao Z (2013) A recursive least squares-based demodulator for electrical tomography. *Rev Sci Instrum* 84(4):044704
- Sun S et al (2017) Digital recursive demodulator based on Kalman filter. *IEEE Trans Instrum Meas* 66(12):3138–3147
- Sun S et al (2014) A high-speed electrical impedance measurement circuit based on information-filtering demodulation. *Meas Sci Technol* 25(7):075010
- Gonzalez-Nakazawa A, Gamio JC, Wuqiang Y (2005) Transient processes and noise in a tomography system: an analytical case study. *IEEE Sens J* 5(2):321–329
- Gamio JC, Yang WQ, Stott AL (2001) Analysis of non-ideal characteristics of an ac-based capacitance transducer for tomography. *Meas Sci Technol* 12(8):1076–1082
- Karali M et al (2018) A new capacitive rotary encoder based on analog synchronous demodulation. *Electr Eng* 100(3):1975–1983
- Yusuf A, et al. (2016) A digital signal processing algorithm on read out circuit for electrical capacitance tomography. In: 2016 IEEE region 10 conference (TENCON)
- Zhou H et al (2013) A complex programmable logic device-based high-precision electrical capacitance tomography system. *Meas Sci Technol* 24(7):9
- Cui Z et al (2011) A high-performance digital system for electrical capacitance tomography. *Meas Sci Technol* 22(5):055503
- Bhat A (2012) Stabilize Your Transimpedance Amplifier. 2012 July 26, 2019]. <https://www.maximintegrated.com/en/app-notes/index.mvp/id/5129#>
- Asparuhova KK, Gadjeva ED (2004). Noise analysis of operational amplifier circuits using MATLAB. In: 27th international spring seminar on electronics technology: meeting the challenges of electronics technology progress, 2004
- Op Amp Noise Relationships: 1/f Noise, RMS Noise and Equivalent Noise Bandwidth MT-048 Tutorial 2009. <https://www.analog.com/media/en/training-seminars/tutorials/MT-047.pdf>
- Lin D-Y et al (2007) Practical and simple circuitry for the measurement of small capacitance. *Rev Sci Instrum* 78(1):014703

35. High Performance, 145 MHz FastFET Op Amps. (2019) Analog Devices. https://www.analog.com/media/en/technical-documentation/data-sheets/AD8065_8066.pdf
36. Precision, High-Speed Transimpedance Amplifier (2019) Texas instruments: <http://www.ti.com/lit/ds/symlink/opa380.pdf>
37. MHz Ultra-Low Bias Current FET Input Op Amp. (2019) Linear technology. <https://www.analog.com/media/en/technical-documentation/data-sheets/62689f.pdf>

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