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Enhanced control method for voltage regulation of DSTATCOM based SEIG

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Abstract

Self-excited induction generator (SEIG)-based wind energy conversion systems (WECS) are very popular for feeding stand-alone loads in remote areas where there is no grid. SEIG needs adjustable reactive power to regulate terminal voltage and frequency. Usually, a combination of a distributed static compensator (DSTATCOM) and a fixed capacitor bank is used to meet this reactive power demand. DSTATCOM is the most suitable option for power quality compensation. The performance of DSTATCOM depends on its control algorithm that generates the proper switching signals for voltage source inverter (VSI). Many control algorithms have been proposed for DSTATCOM in the literature. Among them, the most frequently used algorithms are synchronous reference frame (SRF), instantaneous reactive power (IRP), and current synchronous detection (CSD) algorithms. An effective control algorithm must accurately estimate the amplitude of the terminal voltage without being affected by harmonics, DC-offset, and frequency variation. For this purpose, an enhanced phase locked loop (EPLL)-based CSD control algorithm is proposed to estimate the amplitudes of individual phase voltages, and to filter SEIG voltages in case of harmonics, DC offset, and frequency variation. The proposed algorithm has been tested under linear and nonlinear load conditions. The obtained results clearly demonstrate the effectiveness of the proposed EPLL-based CSD control algorithm.

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Keywords: DC Offset; Distributed static compensator (DSTATCOM); EPLL; Self excited induction generator (SEIG); Wind energy conversion systems (WECS)

1. Introduction

Various generators are used to convert wind energy into electrical energy. Induction generators are widely used in the construction of off-grid wind turbines thanks to the advantages of their easy maintaining, cheapness, and not needing a grid [1]. However, in off-grid electrical systems, the reactive power needed for the induction generator is supplied by the AC capacitor groups connected to the stator terminals. The terminal voltage and frequency of

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SEIG vary depending on the wind speed, the type of loads applied to the system, and the terminal capacitance [2]. Variable capacitance is needed under all load conditions, from no load to full load, to keep the terminal voltage of the SEIG constant [3]. This demand can be met by passive or active compensation components [4,5]. These systems are cost effective and easy to implement, but they are greatly affected by the nature of the load [6]. Therefore, an active var source is used that can provide variable reactive power [7,8].

Power electronics converter-based static var compensation (SVC) and DSTATCOM systems are widely used to provide this reactive power in SEIG applications [9–13]. The use of the DSTATCOM system has come to the fore thanks to the developments in fast power electronic switches such as IGBTs and MOSFETs. The performance of DSTATCOM is superior to SVC, and it does not inject harmonics into the system unlike SVC. Also, its dynamic response is better than SVC [6].

Various control algorithms for DSTATCOM have been reported in the literature [14,15]. In order to improve the terminal voltage, a PI control scheme is presented that produces a reference current by measuring the voltage and current of the generator [16]. This control scheme suffers from instability as it does not take load currents into account to produce the reference currents. Also, DC-offset conditions are not considered. In [9], a control algorithm including a linear second-order regulator is proposed to regulate the terminal voltage and frequency of SEIG under the balanced load conditions. In this control algorithm, if the initial values cannot be selected appropriately, the algorithm works incorrectly. In [11], the SEIG terminal voltage and the STATCOM DC-link voltage are regulated using a fuzzy logic based PI controller. PI coefficients are optimized against wind speed and load variations. The performance of the control scheme to nonlinear loads and DC-offset has not been considered. In [12], the DC bus voltage of STATCOM is controlled by a sliding mode control (SMC) algorithm. The SEIG terminal voltage is regulated by a PI controller. Since hysteresis current control is used to generate PWM signals in the control scheme, it causes a wide variation in switching frequency and higher switching losses. The response of the system in case of DC-offset in load currents and terminal voltages has not been investigated. In [6], the modified current synchronous detection (CSD) algorithm is proposed to control the voltage of SEIG. This method includes a second-order generalized integrator (SOGI) to filter the measured SEIG voltages and estimate the amplitudes of the individual phase voltages. The performance of SOGI under nonlinear loads and DC-offset conditions is insufficient. An effective control algorithm must accurately estimate the phase angle, frequency, and amplitude of the SEIG voltages [17–19].

In this study, an EPLL-based CSD control algorithm is proposed for SEIG-DSTATCOM applications, which eliminates harmonics caused by nonlinear load and DC-offset that may occur due to measurement errors. In the proposed control algorithm, for the estimation of SEIG terminal peak voltage, SEIG phase voltages are filtered with EPLL, and their amplitudes are estimated separately. The harmonic level of the estimated peak amplitude is minimized by a moving average filter (MAF). Also, a delayed signal cancellation (DSC) operator is proposed to prevent the negative effects of DC-offsets in the measured SEIG voltages and load currents. Moreover, the MAF is used to prevent the control algorithm from being affected by the harmonics in the load currents. Thus, it is got rid of the signal delay disadvantage of the low pass filter (LPF) used in the literature. The obtained results clearly demonstrate the superiority of the proposed EPLL-based CSD control algorithm.

2. SEIG-DSTATCOM structure

The schematic diagram of the SEIG-DSTATCOM system feeding the three-phase loads is given in Fig. 1. A star-connected three-phase capacitor bank is connected in parallel to the SEIG terminals so that the SEIG is excited to generate voltage before DSTATCOM is activated. The values of these capacitors are adjusted to obtain the rated voltage at no load. DSTATCOM is connected to the point of common coupling (PCC) via filter inductors to regulate the system voltage that changes as SEIG is loaded. DSTATCOM consists of an IGBT-based VSI and a DC capacitor. DSTATCOM regulates the terminal voltage by providing the total reactive power demanded by the load and the extra reactive power needed to maintain the SEIG terminal voltage. In addition, it provides the necessary current so that the harmonic current drawn by the load does not disturb the SEIG current. Thus, SEIG current and voltage are produced at the desired reference value without being affected by the load.

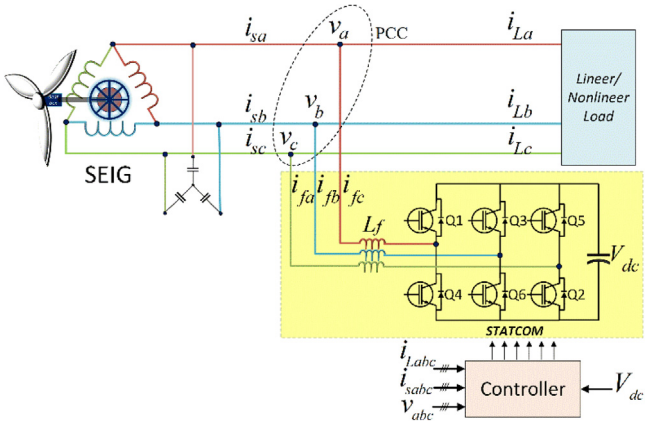

Fig. 1. SEIG-DSTATCOM Structure.

3. EPLL-based CSD control algorithm

The block schematic of the proposed EPLL-based CSD method is shown in Fig. 2. The proposed CSD technique operates three individual EPLL algorithm to extract the peak amplitudes of phase voltages. The structure of single-phase EPLL [20,21] is demonstrated in Fig. 3. The EPLL is a non-linear system that consists of an adaptive band-pass filter (BPF) and a PLL. As illustrated, a phase voltage v_i (here, $i = a$, b, or c) is filtered by the BPF, and v_i' is determined. Note that v_i and v_i' are in same phase.

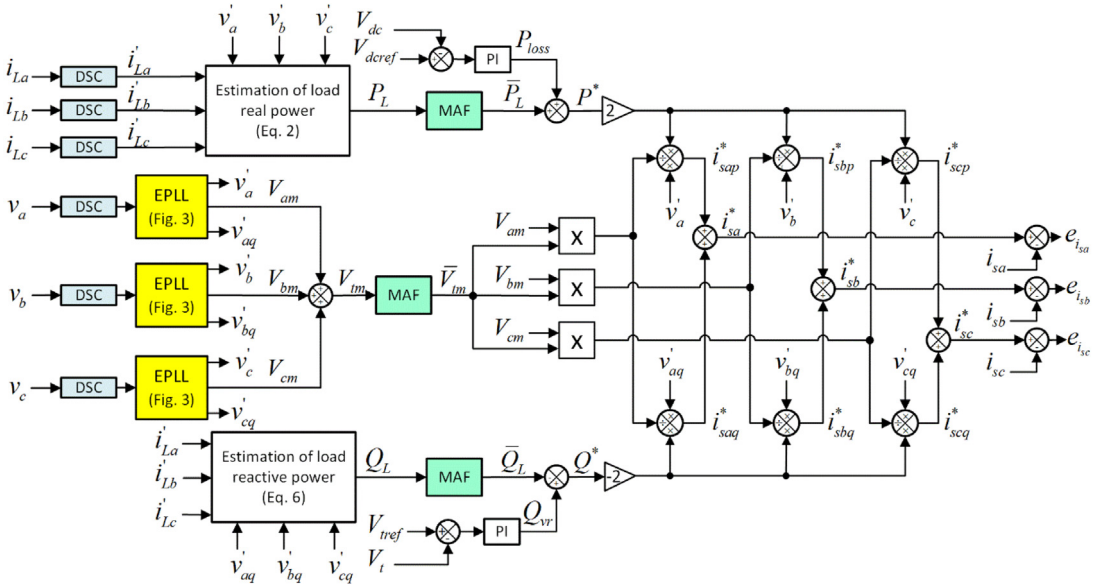

Fig. 2. EPLL-based CSD method.

A 90-degree lagging-phase of v_i (v_{iq}') is obtained by a simple mathematical operation as seen in Fig. 3. Furthermore, the EPLL directly gives the peak value of phase voltage (V_{im}). The error signal (e) is passed through the PLL to estimate the phase-angle and frequency of phase voltage. Notice that the EPLL has its own frequency estimation tool. Thus, even if the SEIG frequency drifts from its nominal value, the EPLL shows a high filtering capability under unbalanced and non-linear loads.

As shown in Fig. 2, the proposed CSD method has three MAFs and three DSC operators. The MAF on the EPLL path assists the EPLL in more accurate estimation of total peak value of phase voltage (V_{tm}). The other two MAFs

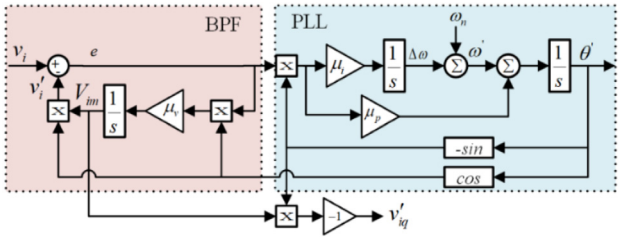

Fig. 3. Schematic of EPLL.

filter out the P_L and Q_L. It is well-known that standard CSD method uses the low-pass filters to filter out the P_L and Q_L [6,22]. The delays caused by the low-pass filters are minimized by using the MAFs in the CSD method.

Since the MAF is a linear finite impulse response (FIR) filter, it can act as an ideal low pass filter if suitable conditions guarantee [17]. Its discrete-time definition can be expressed as

$$\mathrm{MAF}(z) = \frac{1}{N_{MAF}} \frac{1 - z^{-N_{MAF}}}{1 - z^{-1}} \tag{1}$$

where $N_{MAF} = T_\omega / T_s$ (N_{MAF} is the order of MAF, T_ω indicates the window-length of MAF, and T_s is the sampling time). The MAF requires a time equivalent to its window length to achieve steady state. So, larger window length reduces the speed of dynamic response [23]. The schematic of MAF is shown in Fig. 4(a). As observed, its structure is quite simple and easy to implement.

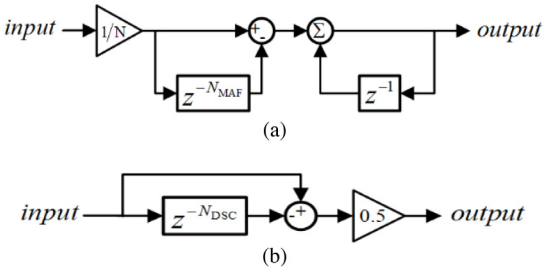

Fig. 4. (a) MAF structure, (b) DSC operator.

As mentioned before, the DC-offset component caused by measurement devices affects the performance of DSTATCOM negatively. To deal with this challenge, a DSC operator for each phase current/voltage is designed. The DSC operator is a FIR filter like the MAF. The block structure of DSC is given in Fig. 4(b), where $N_{DSC} = T/(nT_s)$. In the N_{DSC} equation, T, n, and T_s denote the fundamental period, delay factor, and sampling time, respectively [24,25].

In proposed EPLL-based CSD method, active power of the load (P_L) illustrated in Fig. 2 is calculated as

$$P_L = v'_a i'_{La} + v'_b i'_{Lb} + v'_c i'_{Lc} \tag{2}$$

$i'_{La}, i'_{Lb}, and i'_{Lc}$ are the filtered versions of the load currents. The active power of the load includes DC ($\overline{P_L}$) and AC ($\widetilde{P_L}$) components. SEIG's output power must be free from oscillations to produce quality power. The active power of load is filtered by using MAF as follows

$$\overline{P_L} = P_L - \widetilde{P_L} \tag{3}$$

The reference DC value (V_{dcref}) and the instantaneous value of the DC voltage (V_{dc}) is compared, and the error is entered to PI operator. The output of the PI operator gives the value of P_{loss}. To get the reference active power (P^*) the value P_{loss} is added to the filtered active power of load ($\overline{P_L}$).

$$P^* = P_{loss} + \overline{P_L} \tag{4}$$

The active power components of the reference currents of the SEIG are calculated by using the power expressions in (3) and (4) and the filtered phase voltages (v'_a, v'_bve v'_c).

$$i^*_{sap} = \frac{2P^* v'_a}{\overline{V_{tm}} V_{am}} \; ; \quad i^*_{sbp} = \frac{2P^* v'_b}{\overline{V_{tm}} V_{bm}} \; ; \quad i^*_{scq} = \frac{2P^* v'_c}{\overline{V_{tm}} V_{cm}} \tag{5}$$

The instantaneous reactive power consumed by the load is obtained as

$$Q_L = v'_{aq} i'_{La} + v'_{bq} i'_{Lb} + v'_{cq} i'_{Lc} \tag{6}$$

The instantaneous reactive power of the load (Q_L) may contain oscillation due to the non-linear loads. To produce the reference signals purely, the instantaneous reactive power must be filtered. For this purpose, a MAF is used to extract the DC component of instantaneous reactive power of the load ($\overline{Q_L}$).

$$\overline{Q_L} = Q_L - \widetilde{Q_L} \tag{7}$$

The estimated peak value (V_t) of the SEIG terminal voltages is subtracted from the reference value and the obtained error is entered into the PI operator. The output of the PI controller gives the total reactive power (Q_{VR}) that the system needs to keep constant the SEIG voltage. To obtain the reference reactive power (Q^*) of DSTATCOM, $\overline{Q_L}$ is subtracted from the total reactive power (Q_{VR}).

$$Q^* = Q_{VR} - \overline{Q_L} \tag{8}$$

Using (8) and the fundamental quadrature voltage signals, the reactive power components of the reference currents of the SEIG are obtained as

$$i^*_{saq} = -\frac{2Q^* v'_{aq}}{V_{tm} V_{am}} \; ; \quad i^*_{sbq} = -\frac{2Q^* v'_{bq}}{V_{tm} V_{bm}} \; ; \quad i^*_{scq} = -\frac{2Q^* v'_{cq}}{V_{tm} V_{cm}} \tag{9}$$

As a result, reference currents of SEIG is obtained by summing the active and reactive power components.

$$i^*_{sa} = i^*_{sap} + i^*_{saq} \; ; \quad i^*_{sb} = i^*_{sbp} + i^*_{sbq} \; ; \quad i^*_{sc} = i^*_{sbp} + i^*_{scq} \tag{10}$$

The error signal (e_{isa}, e_{isb} ve e_{isc}) obtained by SEIG reference currents (i^*_{sa}, i^*_{sb}ve i^*_{sc}) and the SEIG actual currents (i_{sa}, i_{sb} ve i_{sc}). is compared with the triangle wave to generate the switching signals for DSTATCOM.

4. Results and analysis

The performance of DSTATCOM with the proposed EPLL-based CSD control algorithm is investigated under various linear and nonlinear load conditions. To prove the effectiveness of the proposed method, SEIG-DSTATCOM is separately tested with both SOGI-based CSD and EPLL-based CSD algorithms under the same conditions. The obtained results under various loads are presented comparatively.

4.1. Performance of SEIG-DSTATCOM under the linear load conditions

Fig. 5 shows the results of the SEIG-DSTATCOM system controlled by SOGI-based CSD and EPLL-based CSD algorithms loaded with a resistive load. In this Fig., the measured load current (i_{La}, i_{Lb}, i_{Lc}), the measured SEIG terminal voltage (v_a, v_b, v_c), the SEIG terminal voltage (*Sogi* v_a, *Sogi* v_b, *Sogi* v_c) and current (*Sogi* i_{sa}, *Sogi* i_{sb}, *Sogi* i_{sc}) of the system controlled by the SOGI-based CSD algorithm, the SEIG terminal voltage (*Epll* v_a, *Epll* v_b, *Epll* v_c) and current (*Epll* i_{sa}, *Epll* i_{sb}, *Epll* i_{sc}) of the system controlled by the proposed control scheme, the SEIG terminal peak voltage (V_t) and the DC Bus voltage (V_{dc}) are shown respectively. At 4 s, the currents that create a DC-offset at the values of −2 A, 3 A, 1 A are added to the load currents, respectively. At 4.15 s, the voltages of −20V, 50 V, 30 V is added to the terminal voltages to create a DC-offset, respectively. Fig. 5(a) shows load currents with a DC-offset added at 4 s and terminal voltages with a DC-offset added at 4.15 s in Fig. 5(b).

In Fig. 5(c), terminal voltages of SEIG-DSTATCOM controlled by SOGI-based CSD algorithm are given. It is seen that the DC-offset added to the currents at 4 s and the voltages at 4.15 s affects the terminal voltage. While there is DC-offset in the load current, a DC-offset of approximately 8 V in each phase of the terminal voltage occurs. When there is DC-offset in both the load current and the measured terminal voltages, a DC-offset of approximately 13 V in each phase of the terminal voltage is reflected. Fig. 5(d) shows the currents of SEIG-DSTATCOM controlled

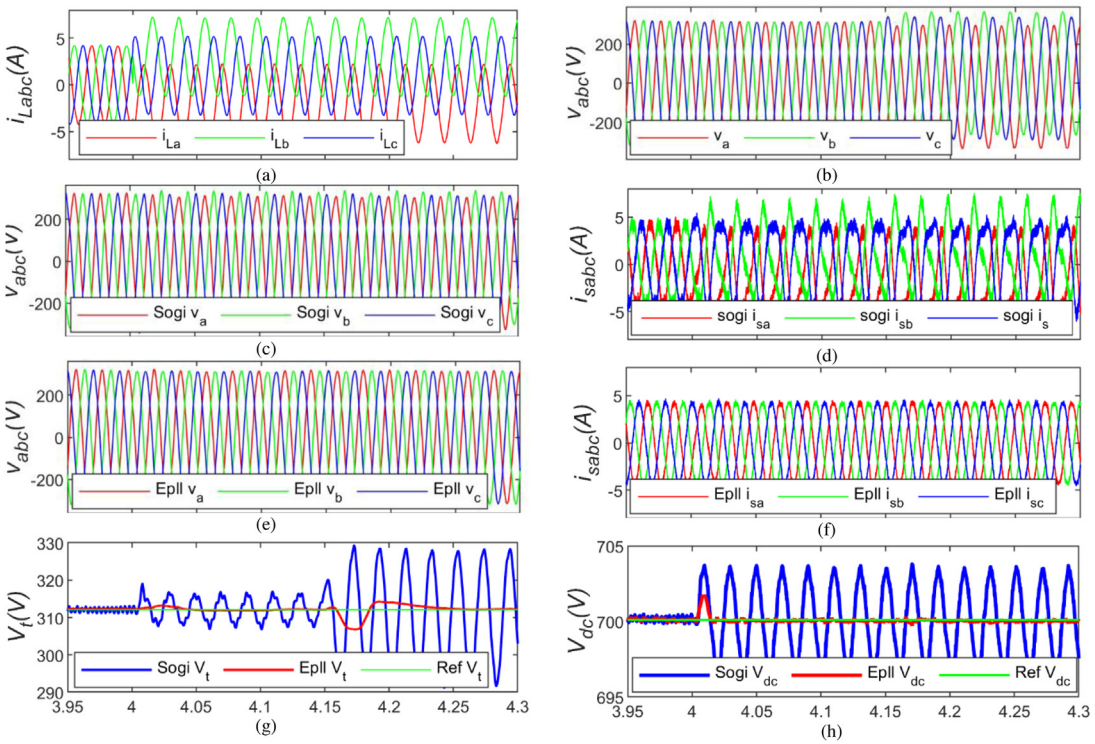

Fig. 5. Linear load (a) Measured load current (b) Measured terminal voltage (c) SEIG voltage (Sogi control scheme) (d) SEIG current (Sogi control scheme) (e) SEIG voltage (EPLL control scheme) (f) SEIG current (Epll control scheme) (g) Terminal peak voltage (h) Dc bus voltage.

by SOGI-based CSD algorithm under the same conditions. While the SEIG current has a DC-offset of 3 A at 4 s, it has a DC-offset of 3.1 A at 4.15 s. As can be seen from Fig. 5, in the presence of DC-offset, the SEIG currents deteriorate considerably.

Fig. 5(e) shows the terminal voltages of SEIG-DSTATCOM controlled by the proposed EPLL-CSD algorithm. As can be seen, thanks to the proposed EPLL-based algorithm, the terminal voltages of SEIG-DSTATCOM are not affected by the DC-offset added to the currents at 4 s and voltages at 4.15 s. Thus, SEIG phase voltages are produced in balanced. The currents of the SEIG controlled by the proposed algorithm are shown in Fig. 5(f). When Fig. 5(d) and Fig. 5(f) are compared, it is clearly seen that the distortions in SEIG currents are corrected when SEIG-DSTATCOM is controlled with the proposed algorithm. As a result, the currents of SEIG-DSTATCOM with SOGI-CSD are highly affected by the DC-offset. Fortunately, the currents of the SEIG-DSTATCOM with EPLL-CSD are almost not affected.

In Fig. 5(g), terminal peak voltages and reference peak voltages of SEIG-DSTATCOM controlled by Epll-based and Sogi-based algorithm are given together. As can be clearly seen, in balanced resistive load conditions (3.95s - 4s), the $EpllV_t$ value is at the reference value; however, the $SogiV_t$ value oscillates between 310.8 V and 313.2 V.

In presence of DC-offset in the load current at 4 s, the V_t value of the SOGI-based method oscillates between 306.9 V-316.5 V, while the V_t value of the EPLL-based method is equal to the reference value without error. In addition to these conditions at 4.15 s, in the case of DC-offset occurring in the terminal voltage, the oscillation of the V_t value (291.6–328.3) in the SOGI-based method is quite high. But V_t value is still at the reference value in the EPLL-based algorithm.

It is important to keep the DC-bus voltage (V_{dc}) at reference values for the stable operation of the system. In Fig. 5(h), V_{dc} values produced by DSTATCOM controlled with EPLL-based and SOGI-based algorithm and reference V_{dcref} value are given on the same axis. It is seen that the $SogiV_{dc}$ value oscillates between 697.9V–704.1 V under DC-offset conditions occurring at 4 s in load currents; however, $EpllV_{dc}$ value tracks the reference value. It is clearly seen that the $EpllV_{dc}$ value is at the reference value in the mentioned conditions. The obtained

results prove that the proposed EPLL-based algorithm is superior to the SOGI-based algorithm under linear load conditions.

4.2. Performance of SEIG- STATCOM under the nonlinear load conditions

Fig. 6 shows the results of the SEIG-DSTATCOM system loaded with a nonlinear load and controlled by SOGI-based and EPLL-based algorithms. Figs. 6(a) and 6(b) show the load currents with a DC-offset at 4 s and the terminal voltages with a DC-offset at 4.15 s, respectively.

In Fig. 6(c), terminal voltages of SEIG-DSTATCOM controlled by SOGI-based algorithm are given under nonlinear load conditions. Only when the load current has a DC-offset, approximately 6.4 V DC-offset is reflected to each phase of the terminal voltage. When DC-offset occurs at the measured terminal voltages in addition to the load currents, approximately 7.3 V DC-offset is reflected to each phase of the SEIG terminal voltage.

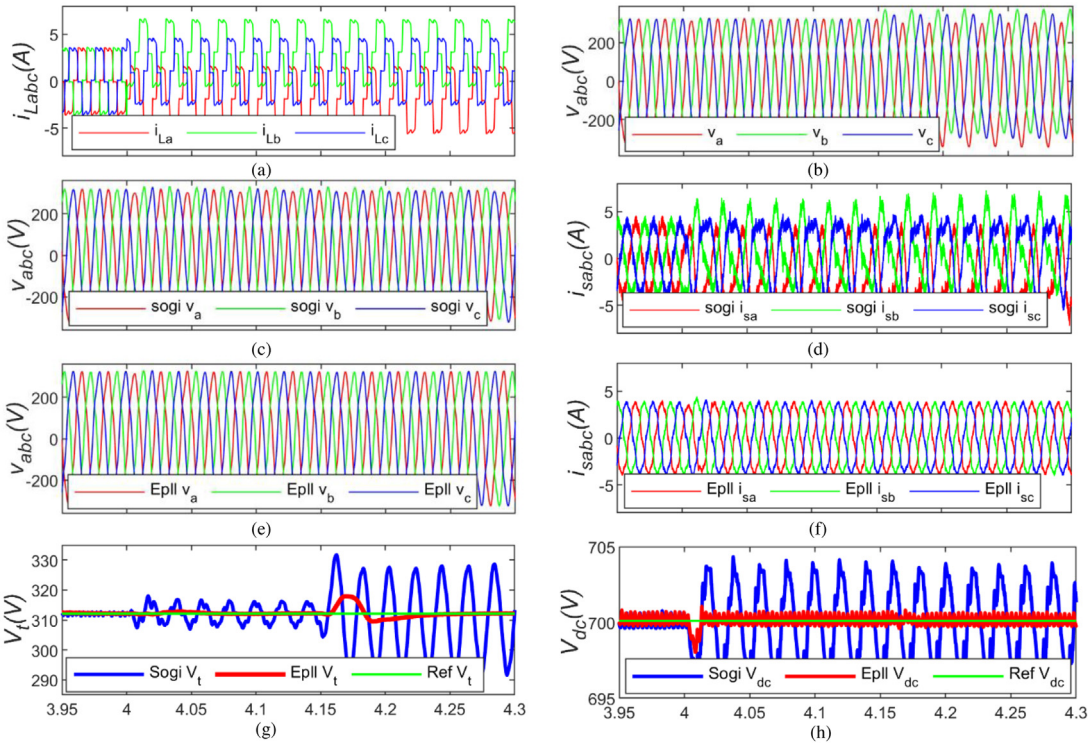

Fig. 6. Nonlinear load (a) Measured load current (b) Measured terminal voltage (c) SEIG voltage (Sogi control scheme) (d) SEIG current (Sogi control scheme) (e) SEIG voltage (EPLL control scheme) (f) SEIG current (Epll control scheme) (g) Terminal peak voltage (h) DC Bus voltage.

Fig. 6(d) shows the SEIG currents of SOGI-CSD under the same conditions. After 4 s the SEIG current has a DC-offset of 2.8 A, while after 4.15 s it has a DC-offset of 3.5 A. As can be observed, the SEIG currents deteriorate considerably due to the DC-offset.

Fig. 6(e) shows the terminal voltages of SEIG-DSTATCOM with the proposed EPLL-CSD. As can be illustrated, the SEIG terminal voltages become balanced and harmonic-free without being affected by the DC-offset.

The currents of the SEIG with proposed EPLL based algorithm are shown in Fig. 6(f). When the SEIG currents produced in Fig. 6(d) and Fig. 6(f) are compared, it is clearly seen that the distortions in the SEIG currents are corrected when the SEIG-DSTATCOM is controlled with the proposed algorithm. As a result, while the currents of the SEIG-DSTATCOM with the SOGI-CSD are highly affected by the DC-offset in the system loaded with nonlinear load, that of EPLL-CSD are almost not affected.

In Fig. 6(g), the generated peak voltages and reference peak voltages in EPLL-CSD and SOGI-CSD are given together. As can be understood from this figure, the *Sogi* V_t value oscillates between 311.2 V and 312.8 V in

nonlinear load conditions (3.95s - 4s), while the *Epll* V_t value is at the reference value. In the case of DC-offset occurring in the load current at 4 s in the nonlinear load applied system, the V_t value of the SOGI-CSD oscillates between 306.9 V – 316.8 V. The V_t value of the EPLL-CSD is equalized to the reference value within a few cycles. At 4.15 s, although the oscillation of the V_t value (290.2–327.8) increases in the SOGI-CSD, the V_t value of the EPLL-CSD is still at the reference value under the same conditions.

In Fig. 6(h), reference V_{dcref} *value* and V_{dc} values produced by SEIG-DSTATCOM controlled with EPLL-based and SOGI-based algorithm are given on the same axis. It is seen that the *Sogi* V_{dc} value oscillates between 697.2V–704.3 V at 4 s; however, the oscillation of *Epll* V_{dc} value is limited to 1 V. It can be clearly seen that the *Epll* V_{dc} value has a very small oscillation of 1 V under the same conditions.

As a result, in SEIG-DSTATCOM applications, it has been proven that the proposed EPLL-based algorithm eliminates harmonics caused by nonlinear load and errors caused by DC-offset much better than the SOGI-based algorithm.

5. Conclusions

In this paper, an EPLL-based CSD control algorithm is proposed for DSTATCOM control and implemented for SEIG voltage regulation. To eliminate harmonics in terminal voltages due to linear loads, the peak amplitudes of phase voltages are estimated separately for each phase by using the EPLL. The obtained peak voltage is passed through the MAF, which is known for its superiority in harmonic elimination, and the harmonic level is minimized. The delay caused by LPF in standard CSD method is reduced by using MAF instead of LPF to filter the load currents. Besides, the DSC operators eliminate the measurement errors that cause the DC-offsets. The performances of the proposed EPLL-based CSD control algorithm and the SOGI-based CSD control algorithm used in the literature are compared. Although there are quite high harmonics and DC-offsets in the currents and voltages of SEIG, the proposed algorithm eliminates these disturbances effectively. In addition, the voltage of the DSTATCOM capacitor is kept constant at the reference value. The results clearly illustrate the superiority of the proposed EPLL-based CSD method over SOGI-based CSD method.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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